Characteristics improvement of top-gate self-aligned amorphous indium gallium zinc oxide thin-film transistors using a dual-gate control

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***Abstract* —** In this work, we have reported dual-gate amorphous indium gallium zinc oxide thin-film transistors (a-IGZO TFTs), where a top-gate self-aligned TFTs has a secondary bottom gate and the TFT integration comprises only five mask steps. The electrical characteristics of a-IGZO TFTs under different gate control are compared. With the enhanced control of the channel with two gates connected together, parameters such as on current (I_{ON}), sub-threshold slope (SS^{-1}), output resistance, and bias-stress instabilities are improved in comparison with single-gate control self-aligned a-IGZO TFTs. We have also investigated the applicability of the dual-gate a-IGZO TFTs in logic circuitry such as 19-stage ring oscillators.

Keywords — *metal oxide, a-IGZO, TFT, self-aligned, dual gate, display technology.*
DOI # 10.1002/jsid.558

1 Introduction

In recent years, amorphous oxide semiconductors, particularly amorphous indium gallium zinc oxide (a-IGZO), have received great interest for thin-film transistor (TFT) applications. They have been investigated as an alternative to amorphous silicon and low-temperature polycrystalline silicon TFTs for active matrix liquid crystal displays and active matrix organic light emitting diode displays and also finding applications in the circuitry such as shift resistors, level shifters, buffers, drivers, and dc–dc converters.[1–6] The a-IGZO characteristics, such as high electron mobility, large area uniformity, and their ability to be fabricated at low temperatures on plastic substrates, are attractive for manufacturing the next generation large area display backplanes and circuits. For performance enhancement of the TFT-based electronic systems, high-speed operation is required. High mobility material and the channel length (L) shrinking are the common way to improve the performance. In TFT configuration for high performance, coplanar self-aligned (SA) gate configuration with zero overlap capacitance (gate-source/drain overlap) is preferred compared with staggered bottom-gate (BG) (back-channel-etch and etch-stop-layer) configuration.[7–15] Another way to achieve the high performance is by the dual-gate (DG) control. Few groups have reported the realization of a-IGZO TFTs with DG control in both staggered (back-channel-etch and etch-stop-layer) and coplanar (standard and SA) configurations, where the top-gate (TG) and BG are electrically connected to each other.[16–25] It is shown that much better control of the channel is achieved which resulted in improved characteristics, that is, higher apparent mobility, higher on-current (I_{ON}), steeper sub-threshold slope (SS^{-1}), and a turn-on voltage (V_{ON}) closer to zero volts. Most of the reported work in DG TFTs is with BG TFT structure where the parasitic capacitance issue due to gate and source/drain (S/D) overlap is not addressed. In other reported work with coplanar SA TG TFT structure, the total number of mask steps used are six or more, where two separated mask steps are required for contacting top gate and bottom gate.[28] In this work, we have demonstrated SA TG a-IGZO TFTs with an additional BG using five mask steps only, thus reducing one mask step. The detailed improvement of the transfer characteristics, their uniformity (across the substrate and substrate to substrate), and channel length independence, V_{ON} close to zero (the desirable parameters for the robust circuits), is demonstrated under DG operations.

2 Experimental

The schematic cross-sectional view of process integration and SEM image of DG TFT are shown in Fig. 1(a) and 1(b), respectively. In the first step, a buffer layer is deposited on the glass substrate. On the top of the buffer layer, a BG metal [MoCr deposited by physical vapor deposition (PVD)] is deposited and patterned. This is followed by deposition of first gate dielectric deposition (SiO_2 by plasma enhanced chemical vapor deposition (PECVD) at 350°C). In the next

Received 12/31/16; accepted 04/27/17.
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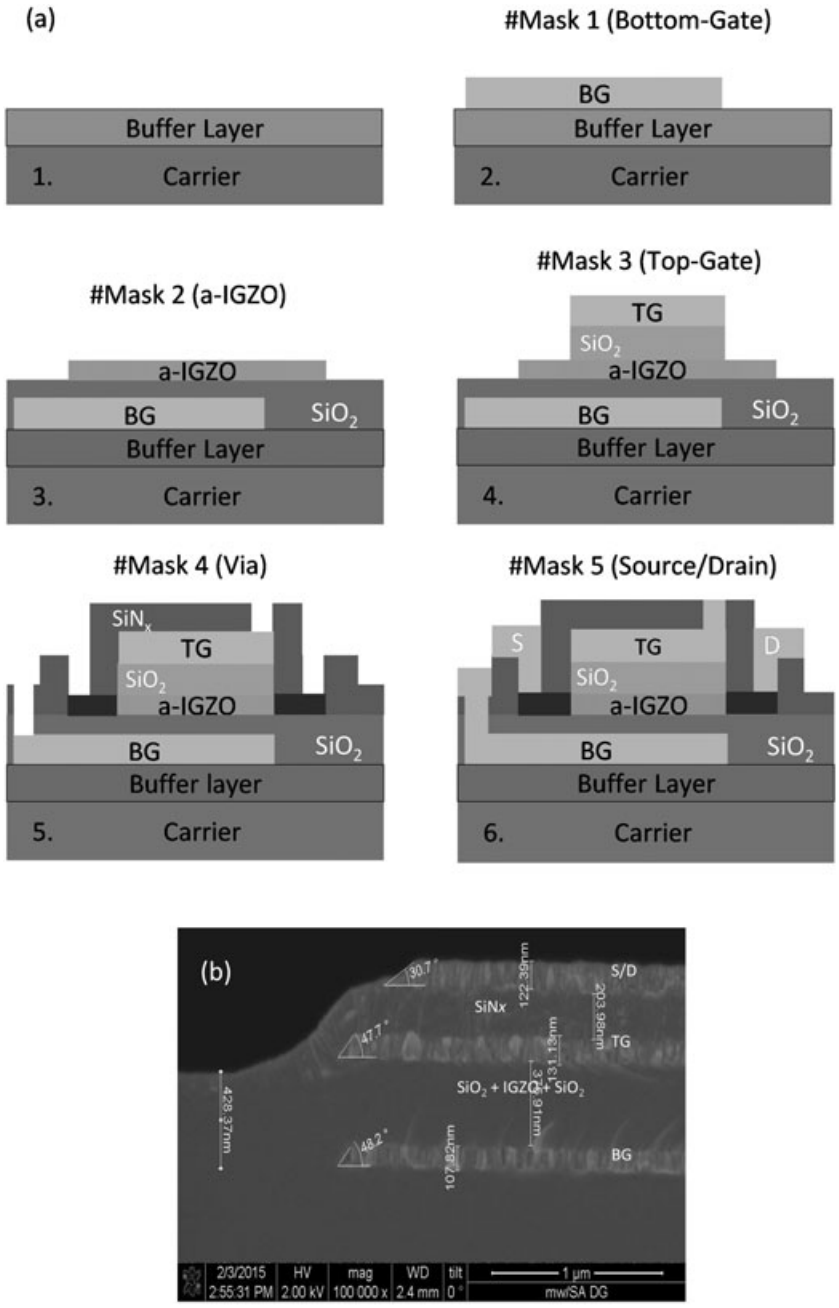

FIGURE 1 — (a) Cross-sectional view of the complete process flow and (b) final SEM view of dual-gate thin-film transistors. BG, bottom gate; TG, top gate.

step, a-IGZO layer (20 nm with 10% ratio of O_2/Ar) is deposited by dc sputtering (PVD) and then patterned using wet etch. Furthermore, it is followed by the deposition of the second gate dielectric (SiO_2 deposition by PECVD at 250°C) and the second gate metal layer (MoCr). In the next step, the gate stack (metal and dielectric) was patterned using combined step of wet and dry etch. Subsequently, an interlayer dielectric (SiN*x* by PECVD at 250°C) is deposited. The contact vias are patterned in the next step using a dry etch process. This contact opening step is combined for contacting the BG metal, TG metal, and S/D regions (#Mask 4). This saves one mask step compared with the earlier reported work on DG TFTs,[27–35]. In the last step, the S/D metal (Mo deposited by PVD) was deposited and then patterned using dry etch. Finally, the samples were annealed at 240°C in the N_2 oven for 1 h. All layers have been patterned using standard photolithography techniques, and all the processes were performed at a temperature below 350°C to enable integration on polyimide foil and a range of potential moisture barriers.[26] The electrical characteristics of the individual TFTs and inverters were measured using a parameter analyzer (Agilent 4156) in N_2 environment. The output characteristics of the ring oscillators were examined with an oscilloscope.

3 Results and discussion

In coplanar SA TFT configuration, the sheet resistance (R_{SHEET}) of the spacing region (SP region between gate and S/D as shown in Fig. 1(a)) and contact resistance ($R_{CONTACT}$) are important factors. They are responsible for limiting the trans-conductance and hence the channel mobility.[14,15] SiN*x* interlayer (a-IGZO doping due to high hydrogen content of the layer) has been utilized to change the conductivity of the SP region. The contact resistance, $R_{CONTACT} = R_S + R_D$, with R_S and R_D respectively the source and drain resistances, and sheet resistance (R_{SHEET}) were extracted using the transfer length method. The utilized transfer length method structure contained nine TFTs with fixed channel width (W = 250 μm) and varying channel length (L = 10–100 μm) values from the width normalized contact resistance $R_{CONTACT}.W$ value versus channel length L plot as shown in Fig. 2. The R_{SHEET} value of ~1.1 kΩ/□ is obtained. This value is lower enough for the DG TFT's integration in our large-scale applications.

Typical transfer and output characteristics of the TFTs (W/L = 15/5 μm/μm) with TG, BG, and DG controls are shown in

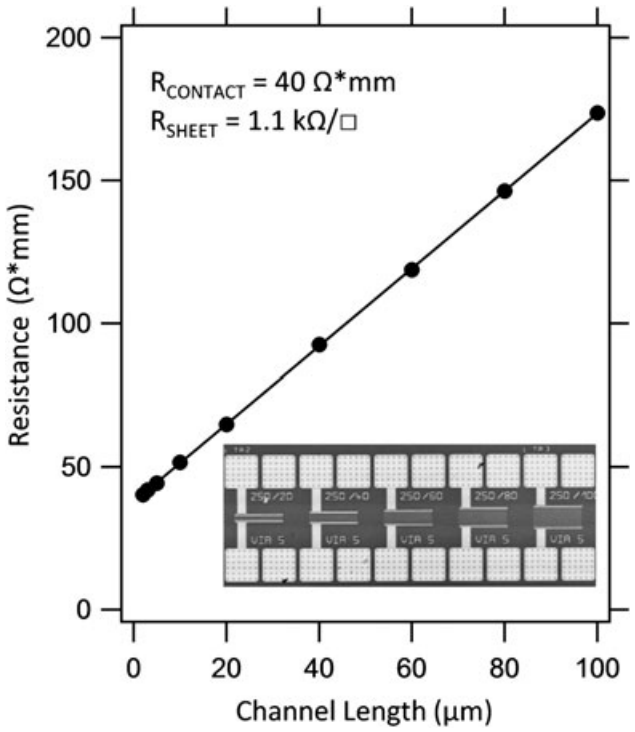

FIGURE 2 — The transistor resistance as a function of channel length '*L*' for dual-gate thin-film transistors with SiN*x* interlayer. The contact resistances are obtained from the extrapolation to a zero channel length. The layout of contact layout is shown in the inset.

TABLE 1 — Comparison of amorphous indium gallium zinc oxide thin-film transistor characteristics at different operation conditions for V_{GS} values between −20 and 20 V and V_{DS} value of 20 V.

Parameters	Bottom gate	Top gate	Dual gate	Isolated top gate
μ_{FE} (cm^2/V.s)	10.3	9.3	20.6	9.0
V_{ON} (V)	−4.0	−3.5	0	−10.5
SS^{-1} (V/dec)	0.38	0.37	0.28	0.70
I_{ON}/I_{OFF}	9.40×10^7	5.60×10^7	1.80×10^8	1.70×10^8

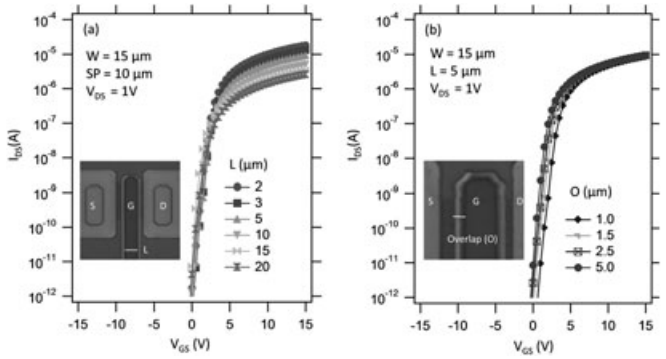

FIGURE 4 — Self-aligned thin-film transistor's transfer characteristics (V_{GS} between −15 and 15 V and a V_{DS} value of 1 V) dependence on (a) channel length '*L*' (SP = 10 μm) and (b) gate overlap 'O'.

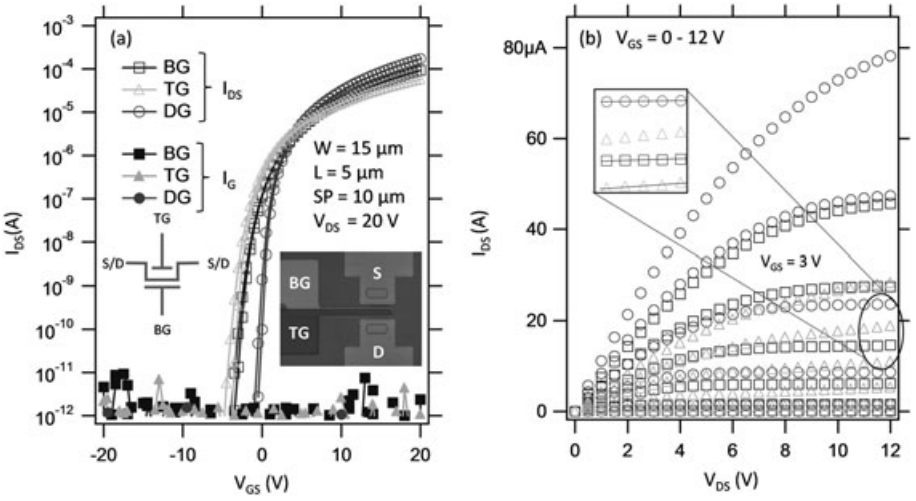

FIGURE 3 — (a) Transfer (at V_{GS} between −20 and 20 V and a V_{DS} value of 20 V) and (b) output characteristics (at V_{DS} of 0 to 12 V and V_{GS} between 0 and 12 V) of dual-gate thin-film transistors (DG TFTs). Layout of the thin-film transistor is shown in the inset. BG, bottom gate; TG, top gate.

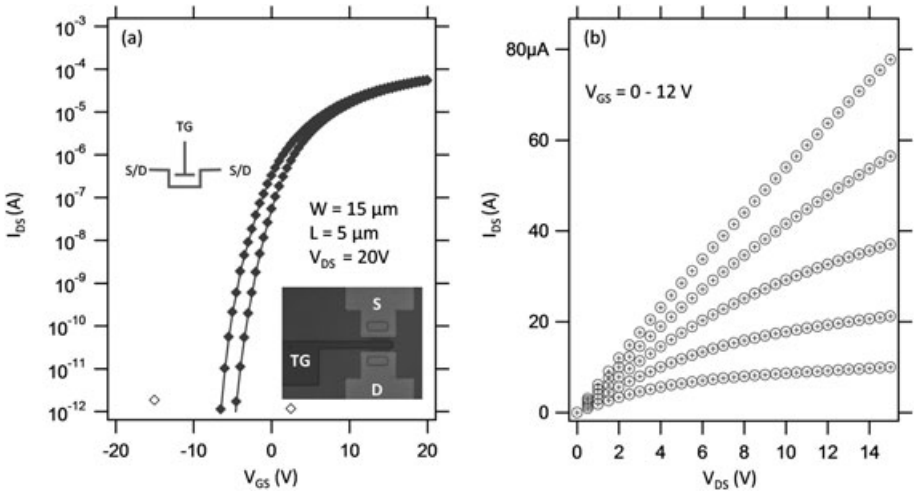

FIGURE 5 — (a) Transfer (at V_{GS} between −20 and 20 V and a V_{DS} value of 20 V) and (b) output characteristics (at V_{DS} of 0 to 12 V and V_{GS} between 0 and 12 V) of top-gate self-aligned thin-film transistors. Layout of the thin-film transistor is shown in the inset.

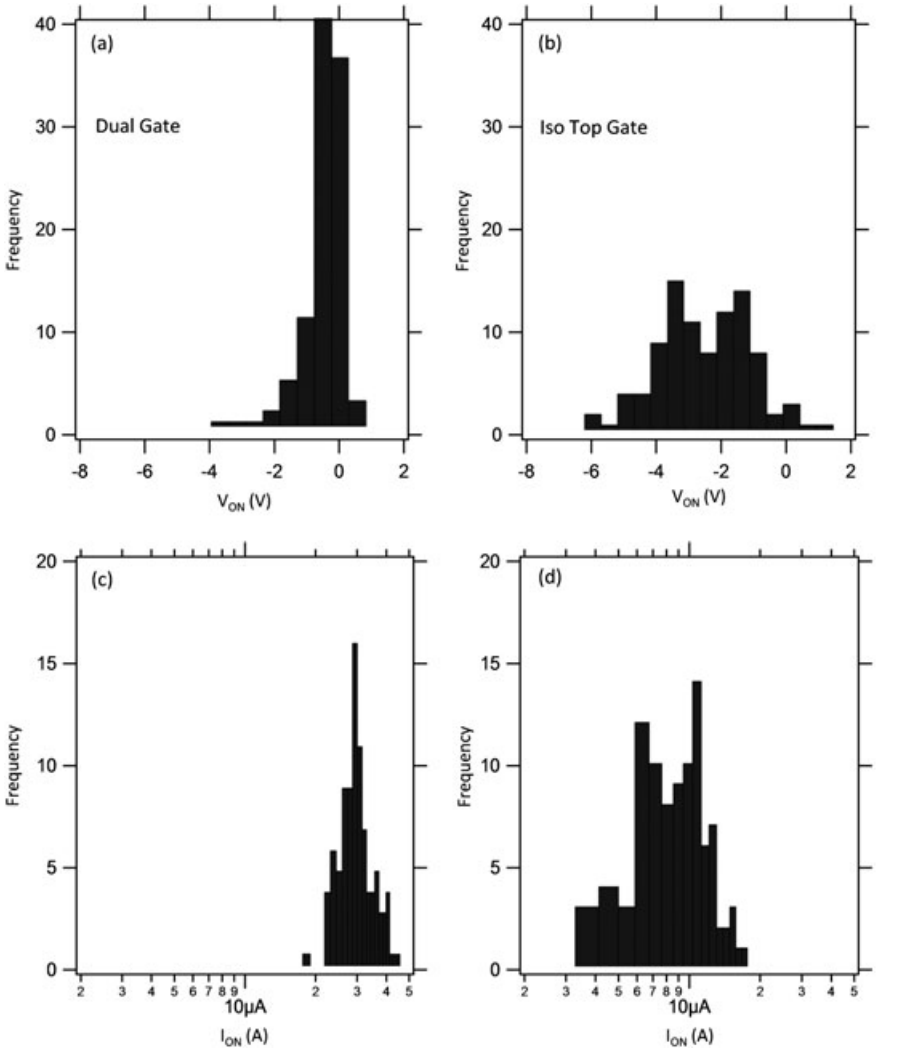

FIGURE 6 — Histogram of V_{ON} and I_{ON} for 100 amorphous indium gallium zinc oxide-isolated top-gate and dual-gate thin-film transistors.

Fig. 3(a) and 3(b), respectively. The microscope image of the TFT is also shown in Fig. 3(a) (inset view). Figures of merit of these TFTs at a drain-to-source voltage (V_{DS}) of 20 V are summarized in Table 1. The DG TFTs show apparent mobility (μ_{FE}) of 20.0 cm^2/V.s, SS^{-1} of 0.28 V/decade, and current (I_{ON}/I_{OFF}) ratio of 1.8×10^8. They exhibit over three times increase in I_{ON} and one and a half time steeper value of SS^{-1} when compared with single (top) gate TFTs. The turn-on-voltage (V_{ON}) value of close to zero volts compare with single-gated TFTs is another improvement. The gate leakage current caused by the increased gate area is negligible as well. In output characteristics, no s-shaped behavior is observed at low values of V_{DS}. This means that the S/D regions are nicely doped. Further, the output resistance (change in I_{DS}/change in V_{DS} ($\Delta I_{DS}/\Delta V_{DS}$) at V_{GS} = 3.0 V) is low for the DG TFTs in comparison with the independent TG and BG TFTs. All these improvements are due to the improved control of the channel potential when the two gates are connected together. Furthermore, to verify again that the R_{SHEET} of the gate-source contact is well distributed across the channel spacing and not influencing the channel length, the transfer characteristics of DG TFTs (at V_{DS} = 1 V) with different channel lengths (L = 2, 3, 5, 10, and 20 μm) were compared. The characteristic such as I_{ON} nicely scale with channel length is shown in Fig. 4(a). In another comparison, TFTs with different overlaps (O = 1.0, 1.5, 2.0, and 5 μm, where O is defined as the difference between the channel lengths of the bottom and the top gate) were compared. It is to be noticed that with overlap change, the space region does change between the gate and S/D. This could possibly impact the TFT characteristics if the doping of the space region is not uniform. As shown in Fig. 4(b), no variation of TFT characteristics with different gate overlaps is observed. This clarifies that the spacing region is uniformly doped.

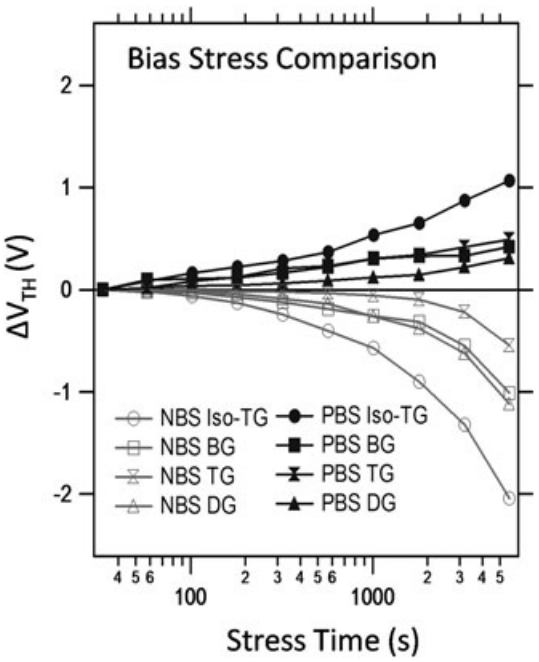

FIGURE 7 — V_{TH} shift as function of stress time under +1 MV/cm (V_{GS}–V_{ON} = +20 V and V_{DS} = 0 V) and under 1 MV/cm (V_{GS}–V_{ON} = ±20 V and V_{DS} = 0 V) field strength in dark at room temperature.

It is also worth mentioning that the improved metallic shielding reduces the impact of buffer layer out-degassing[27] on the TFT characteristics because the isolated TG TFTs (TFTs without physical bottom gate) shows poor TFT characteristics. The typical transfer and output characteristics of these TFTs (W/L = 15/5 μm/μm) are shown in Fig. 5(a) and 5b, respectively. The microscopic image of these TFTs is also shown in Fig. 5(a) (inset view). The characteristics are also listed in Table. 1. It can be seen that a very negative V_{ON} (approximately −6.0 V) and poor SS^{-1} is observed for these TFTs. In output characteristics, similar to DG TFTs, no s-shaped behavior is observed at low values of V_{DS}; however, the output resistance ($\Delta I_{DS}/\Delta V_{DS}$) is high in comparison with the DG TFTs. This is possibly due to poor shielding of

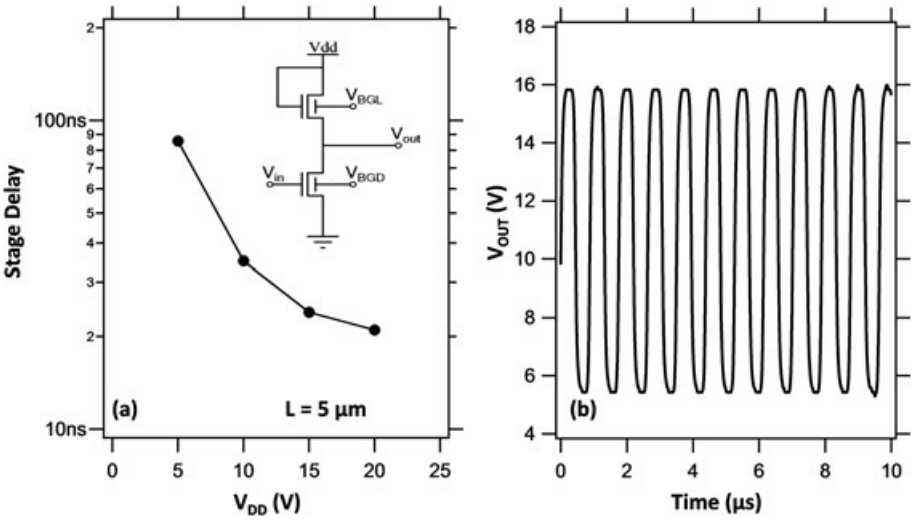

FIGURE 8 — (a) Stage delay versus supply voltage for dual-gate 19-stage ring oscillators, designed in diode-load logic for L = 5 μm (inset; inverter scheme used in this work, whereby V_{BGL} and V_{BGD} are independent biases); (b) output pattern of dual-gate oscillator at V_{DD} = 20 V.

channels from the bottom, a possible impact of buffer layer out-diffusion happened during the final annealing step.[27] In Fig. 6, the statistical plots of V_{ON} and I_{ON} of 100 DG control TFTs (at V_{DS} = 10 V) is compared with isolated TG TFTs. It is observed that both V_{ON} and I_{ON} spread is better for DG control TFTs in comparison with isolated TG TFTs. In another TFT characterization, the bias-stress stability of DG (under different gate control) and isolated TG TFTs with an identical a-IGZO channel is investigated. All the TFTs were stressed at room temperature under +1 MV/cm (V_{GS}–V_{ON}= +20 V and V_{DS} = 0 V) in positive direction and at −1 MV/cm (V_{GS}–V_{ON} = −20 V and V_{DS} = 0 V) in negative direction for a period of 10^4 s. It is observed that the mobility (linear), SS^{-1}, and I_{ON}/I_{OFF} ratio are quite similar before and after the complete stressing experiment for all the TFTs. However, as shown in Fig. 7, a lower threshold voltage (V_{TH}) change of less than 1.0 V (in both positive and negative directions) is observed for the DG TFTs in comparison with isolated TG TFTs. These good results for the DG control TFTs could also be due to the presence of the additional metallic bottom gate that provides better encapsulation to the channel[28–32]

In circuits, the realization of ring oscillator (19-stage) will provide a reliable estimate of the speed of the logic gates that can be made in this technology.[14,15,19,25,29,33–35] The inverter schematic that allows the independent biasing of V_{BGL} (BG load) and V_{BGD} (BG drive) is depicted in the inset of Fig. 8 (a).[33] The resulting stage delay versus the supply voltage of the ring oscillators is plotted in Fig. 8(a). At each measurement point, we have used specific bias voltages for the back gates to obtain the maximum frequency or minimum delay. As an example, at a supply voltage of 20 V, we applied V_{BGD} of 6 V and V_{BGL} of 35 V, which resulted in an oscillation frequency of 1.24 MHz. This corresponds to a stage delay of 20 ns. The voltage output curve of the oscillator at a voltage drain drain (V_{DD}) of 20 V is shown in Fig. 8(b).

4 Conclusion

In summary, the DG a-IGZO TFTs with improved performance and lesser mask steps have been demonstrated. It has been shown that with the DG control, the TFTs have higher I_{ON}, steeper SS^{-1}, lower output resistance, V_{ON} closer to zero volts, and smaller V_{TH} shift under bias stress in comparison with TFTs under single-gate control. We also demonstrated the applicability of these TFTs in logic circuitry.

Acknowledgment

This work was performed in a collaboration between imec and TNO in the frame of the HOLST Centre.

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